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# Low Power Digital CMOS Design

*Anantha P. Chandrakasan, Robert W. Brodersen*

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Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology.
Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible.
The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the $CV^2f$ barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

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